EXPERIMENTAL AND ANALYTICAL INVESTIGATION OF SINGLE EVENT, MULTIPLE BIT UPSETS IN POLY-SILICON LOAD, 64K × 1 NMOS SRAMs

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ABSTRACT

Long time constants associated with extremely high pull-up resistances commonly used in high-density, poly-silicon load NMOS SRAMs have been identified as the primary cause of single-event-induced, multiple bit upsets recently observed in cyclotron tests. Diffusion currents can cause single event errors in this long time constant regime. Above certain threshold LETs, multiple bit upsets constitute almost the entirety of single event errors in these SRAMs. Conventionally calculated error cross-sections can be larger than the chip area and may result in unreasonably large bit error rates. A new method of defining the SEU figure-of-merit in space environments which includes multiple bit upsets is thus urgently needed.

INTRODUCTION

Single event upsets (SEUs) pose serious reliability problems in the space application of VLSI devices. Conventional analyses of SEU have traditionally been based on a probabilistic concept, error cross-sections being defined as the number of bit upsets observed per unit fluence. Implicit to this concept is the existence of a fractional device area which is sensitive to SEU such that the error cross-section would be no larger than the physical cross-section. When a device is so sensitive to heavy ions that every particle hit causes one or more errors, the error cross-section can actually be larger than the physical cross-section. In such cases a concept based on the deterministic relation would be more relevant in describing SEU than a probabilistic one.

We have recently observed in the cyclotron tests of poly-silicon load, 64K NMOS SRAMs a phenomenon very similar to that just described. The dependence of error cross-sections on particle LETs for the device is shown in Figure 1. Data from oblique as well as normal incidences of ions are included. The conventional error cross-section (i.e., number of observed bit-errors per unit fluence) exceeded the physical cross-section as denoted by inverted triangles. This is evidence of multiple bit upsets (MBUs) caused by a single particle hit. When corrected for MBUs, the event cross-section approached the physical device cross-section, indicating 100% SEU probability. The device under investigation represents one of the high speed NMOS SRAM candidates currently under consideration for large space-borne computers at low altitudes. Extremely large error rates as shown in Figure 1 are of serious concern in such applications.

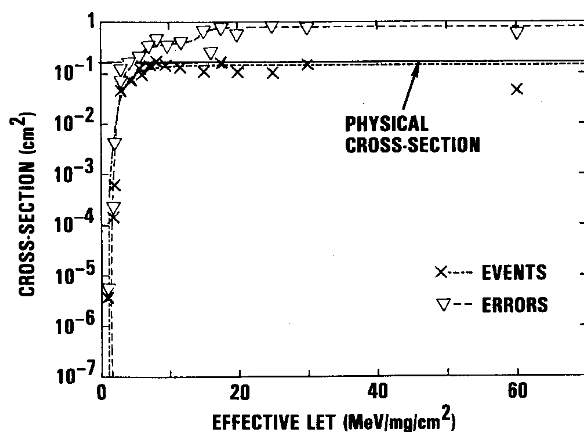

Figure 1. Unprocessed error cross-sections

The extreme SEU sensitivity of this memory cell (shown in Figure 2) stems from the use of a very high pull-up resistance, R_P, on the order of giga-ohms, to maintain the stand-by current at the equivalent-device-density CMOS level [1]. The circuit time constant required to restore a "high" node condition after an SEU hit, for instance, can be extremely large, well on the order of microseconds, due to the high R_P's. In this regime, slow diffusion currents can also contribute to memory upsets. Ions, not directly incident upon sensitive drain areas, can thus cause upsets through diffusion currents. Further, a single ion hit can upset more than one cell, provided that a sufficient LET is delivered [2]. The event cross-sections for MBUs become a measure of the range of diffusion currents and, therefore, are LET-sensitive. Above a certain critical LET, it is possible for the entire chip area to become SEU-sensitive. Furthermore, due to the fine feature sizes associated with these high density NMOS SRAMs, the critical charge Q_C is also extremely small [3].

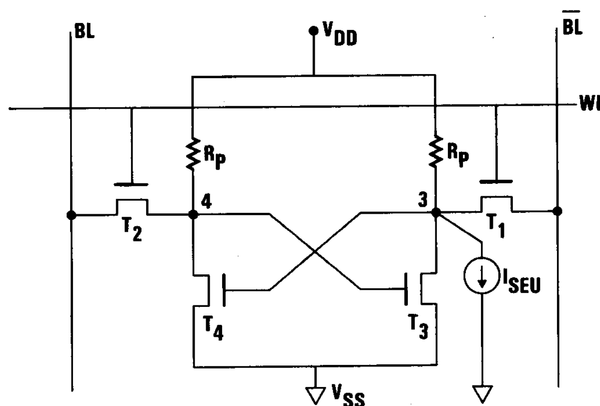

Figure 2. Circuit schematic of memory cell

This paper presents results of experimental and analytical studies of single-event-induced MBUs in a 64K × 1 NMOS SRAM. Experimental methods have been developed to detect and classify the multiplicity of single event errors. Analytical methods have been developed to establish understanding of the MBU phenomena from a device and circuit point of view. The results will aid in developing guidelines for hardening NMOS devices against MBUs, and also in establishing criteria for the device figure-of-merit in the MBU environment.

EXPERIMENTAL

The device studied was one of the currently available, commercial 64K × 1 NMOS SRAMs. The NMOS cells were fabricated in a common p-well. A memory cell consists of four transistors and two poly-silicon pull-up resistors, whose circuit is shown in Figure 2. R_P is typically 1 giga-ohm. The V_{DD} line is doped poly-silicon, and the V_{SS} line buried diffusions. The device READ access time is about 35 ns.

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The SEU experiments were performed at the U. C. Berkeley 88" cyclotron. Ion species of ^{16}O, ^{15}N, ^{20}Ne, ^{40}Ar, and ^{63}Cu with an LET of 1, 3, 6, 15, and 30 MeV/mg/cm^2, respectively, were used. For the error multiplicity resolution, only the normal incidence data were analyzed. The checkerboard was used as the primary test pattern, although all "0's" and all "1's" were also used. The computer-controlled memory exerciser was programmed to read the cells continuously in a series of cycles during the heavy ion bombardment. The READ time was 625 ns for each cell, and 40 ms for a 64K-cell cycle in this experiment. After each cycle of READ, error bits were corrected before the next READ.

TEST RESULTS

Physical Error Bit Maps

Bit error data were decoded using a bit map algorithm to produce physical error maps. When the error cross-section (Figure 1) was smaller than the physical cross-section, the error map was composed mainly of isolated, single bit errors, as shown in Figure 3a for ^{15}N with an LET of 3 MeV/mg/cm^2. Note that occasional double errors were also observed with ^{15}N. However, when the error cross-section (Figure 1) was apparently larger than the physical one, the error map contained predominantly clusters of bit errors, as shown in Figure 3b for ^{40}Ar with 15 MeV/mg/cm^2. Indeed, there are no isolated, single errors on this map. These error maps represent data accumulations from many READ cycles. However, each cluster in Figure 3b was observed during an individual READ cycle. With the ^{40}Ar experiment, as well as with other multiple error experiments, the beam intensity was adjusted sufficiently low to insure that there were many error-free READ cycles with occasional, isolated cycles containing errors.

Multiple Error Cross-Sections

The cross-sections for multiple errors were analyzed in the following way. The error data were analyzed frame by frame after each completion of the READ cycle. For each LET with normal incidence, the probability of SEU was calculated using the Poisson distribution for the fluence in each cycle. The fluence per cycle was kept sufficiently low to have the Poisson-predicted error rate less than one per cycle. When the observed error counts in a cycle were substantially different from the Poisson distribution, they were assumed to represent multiple errors. Error bit addresses were decoded using a bit map algorithm to resolve the clustering of error bits. Multiple-error cross-sections obtained in this way are shown in Figure 4 for the five species of ions, namely ^{16}O, ^{15}N, ^{20}Ne, ^{40}Ar, and ^{63}Cu, at normal incidence only.

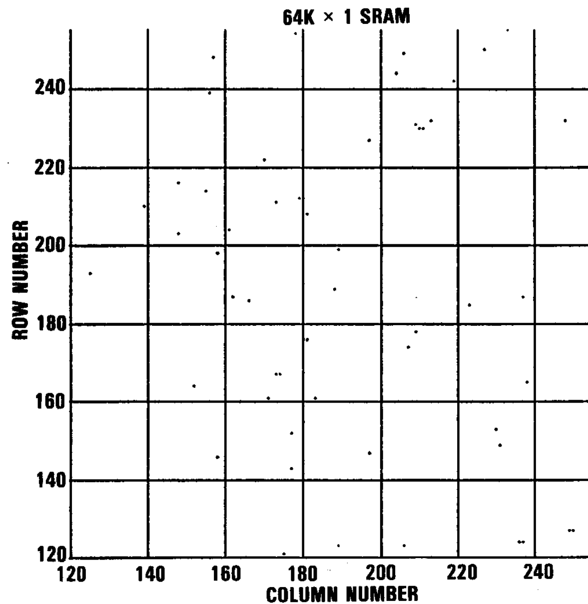

Figure 3a. Error bit map for ^{15}N (Only upper right quadrant shown)

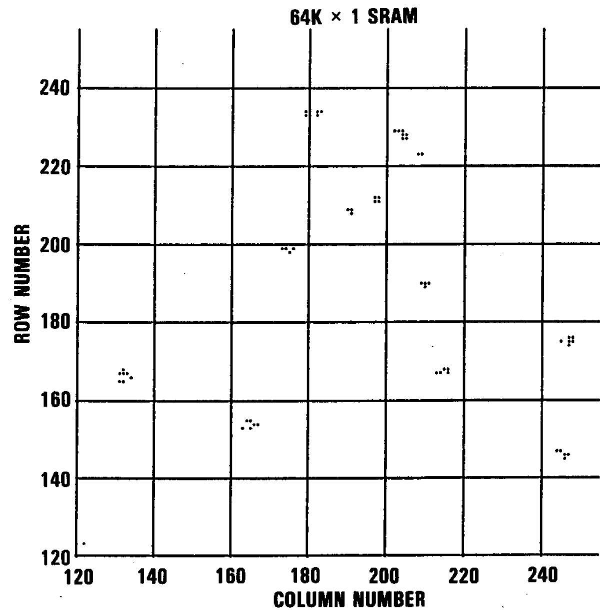

Figure 3b. Error bit map for ^{40}Ar (Only upper right quadrant shown)

A few salient observations can be made from the data: (1) there exists an LET threshold for each multiplicity of errors; (2) thresholds apparently increase with multiplicity; (3) there also exist asymptotic cross-sections for certain multiplicities at large LETs; and (4) as multiple errors dominate, single errors begin to disappear. Since only the normal incidence data were included in Figure 4, the resolution in LETs is somewhat coarse. For instance, data between 1 and 3 MeV/mg/cm^2 are needed for a finer resolution of LET thresholds for multiple errors. Respective multiple error cross-sections, especially at large LETs, do not add up to the total event cross-sections shown in Figure 1. Since Figure 1 does include oblique incidence data, the discrepancy is most probably due to the difference in the spatial extents of diffusion currents corresponding to the different directions of incidence.

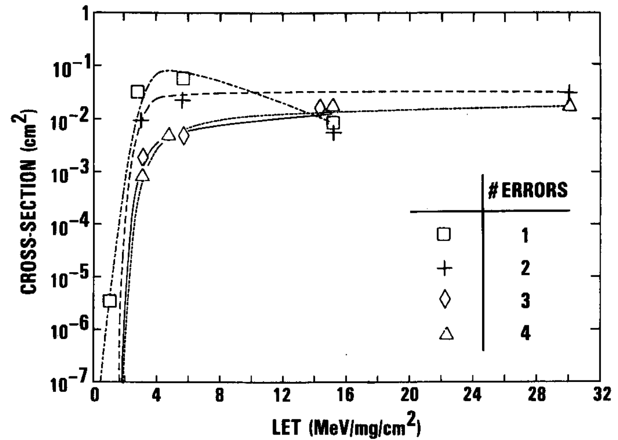

Figure 4. Multiple error cross-sections versus LET

ANALYSIS AND DISCUSSION

PISCES Simulation of SEU Current Pulses

The first step in the analysis was to obtain realistic SEU current pulses to be used in the circuit analysis later. The SEU current pulses at the drain nodes were calculated using the 2-D code PISCES, which

automatically takes care of distributed, non-equilibrium, dynamic charge transport processes using its built-in device physics capability. A rectangular slab in the vertical plane, 10 μm deep and 34 μm wide, was used in the simulation. A simulation depth of 10 μm into the substrate consisting of a 4 μm deep p-well on an n-substrate is expected to provide reasonably accurate charge collection results including funneling. In a typical charge sharing simulation, two n^+ drains and two p^+ substrate contacts were symmetrically laid out with respect to the vertical center line on the top of the rectangle. The drains were inside and the contacts outside with various inter-drain and inter-contact spacings. Ions were incident normally at a point between the drains. The drains and substrate were biased at 5 V, and the p-well at 0 V.

Initial conditions for charge generation from heavy ions were obtained using the Monte-Carlo electron slowing down code TRIPOS-E [4]. Charge generation profiles were fitted to an analytical form consisting of a Gaussian at the center and an exponential toward the outside. The charge density was normalized using the experimentally observed LET thresholds. An SEU current from a direct hit of a ^{15}N ion to a drain is shown in Figure 5a. This type of pulse, which is mostly drift current, was used for a single error analysis. A similar pulse arising from charge sharing between the two nearest cell drains from a ^{40}Ar ion impinging midway between the drains is shown in Figure 5b. The distance from the hit point to drains in this case was 3.9 μm. This type of pulse, diffusion plus drift, was used for multiple error analysis. The pulse-width in Figure 5b was about 4 ns, only twice as long as that in 5a, a direct hit. Memory cells were laid out in a 10 μm × 20 μm lattice on the chip surface for this device. A typical inter-cell distance along the diagonal direction of the lattice is about 22 μm, and the diffusion time for this distance is expected to be at about 100 ns, which is considerably shorter than the estimated circuit response time. The initial excursion of SEU pulses in a negative direction, as shown in Figures 5a and 5b, is due to the dielectric displacement current across the junctions. SEU current pulses were found to be quite sensitive to LETs, but not to initial charge track sizes.

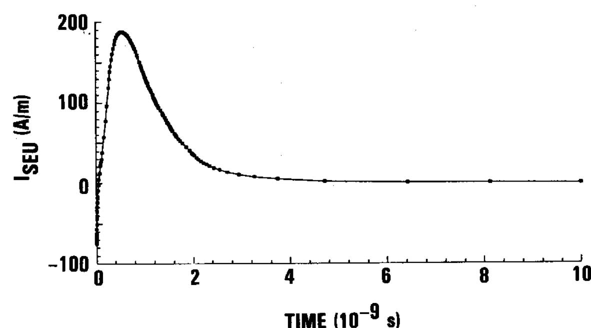

Figure 5a. PISCES SEU current pulse for ^{15}N: direct hit on drain

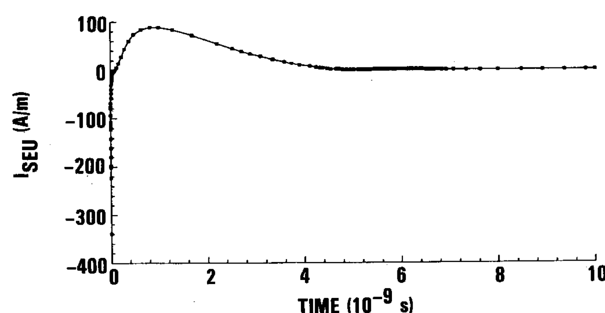

Figure 5b. PISCES SEU current pulse for ^{40}Ar: midway between two drains

SPICE Simulation of Upset

The response of a memory cell to the SEU current pulses obtained above was simulated using the circuit shown in Figure 2. SPICE parameters were calculated from the available layout and process information. The circuit responses resulting in upset and recovery are shown in Figures 6a and 6b, respectively. V_3 was initially high; V_4 low. The criteria for upset are whether V_3 can swing below V_4 and also, V_T, the threshold voltage for T_4. Because of non-negligible gate-to-drain capacitances, voltages on two nodes are easily equalized with fast SEU current pulses. Remaining minute differences between two node voltages determine which transistor reaches the "on" state first. The total charges contained in the current pulses of Figures 6a and 6b were 0.05 pC and 0.04 pC, respectively. Q_C is, therefore, about 0.04 pC for this cell, a value which is considerably smaller than that for similar size CMOS cells. The most important point to note is the long time constant of recovery, which is on the order of microseconds. This makes the circuit vulnerable to long current pulses, viz., the diffusion current from non-direct hits. The long time constant coupled with small Q_C is the primary cause of the prevalence of MBUs for high LET particles. The present experimental data with a READ cycle time of 40 ms precluded the possibility of observing the "single event disturb" effect [1].

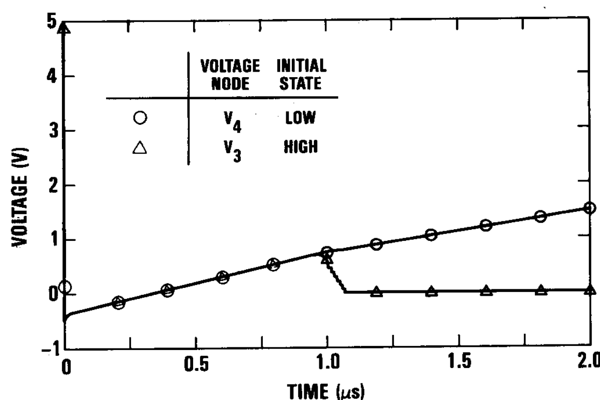

Figure 6a. SPICE simulation resulting in upset: Q = 0.05 pC

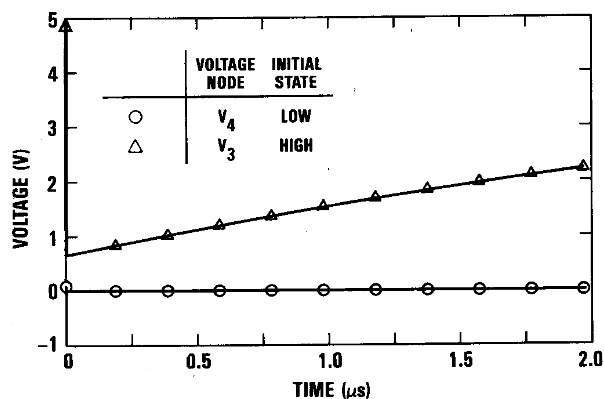

Figure 6b. SPICE simulation resulting in no upset: Q = 0.04 pC

LET Thresholds for MBU

To account for the existence of LET thresholds for MBUs (Figure 4), we have first constructed in Figure 7 curves of collected charge versus

distance between the hit point and the collection node for various LET particles using the PISCES code in the vertical slab geometry as previously discussed in the SEU current calculations. Using the device layout data we have defined critical distances, r_C, for 2-bit and 4-bit errors as the minimum possible distances to two and four adjacent cell drains, respectively, from a single point on the chip. These distances are shown as vertical dashed lines in Figure 7. The horizontal dashed line denotes the critical charge, Q_C, as determined by the SPICE simulation. If a curve for certain ions lies above the intersection of Q_C and the respective r_C, those ions are capable of creating errors of the respective multiplicity by making the drains individually collect charge greater than Q_C. The charge density was normalized from the data of Figure 4 by taking the double error point with a cross-section of 10^{-2} cm^2 at LET of 3 $MeV/mg/cm^2$ (^{15}N) as the threshold for 2-bit errors. This makes the curve for ^{15}N pass through the intersection of Q_C and r_C (= 3.9 μm). As can be seen in Figure 7 with this charge normalization, the threshold for 4-bit errors at LET 15 $MeV/mg/cm^2$ for ^{40}Ar (Figure 4) is in reasonably good agreement with the PISCES simulation. The PISCES simulation seems to predict a slightly lower collected charge than Q_C for ^{40}Ar at r_C = 9.5 μm, the critical distance for 4-bit errors. This points to the well known charge normalization problem in 2-D codes to accurately simulate 3-D problems [5]. Despite these difficulties, the 2-D PISCES does offer valuable capabilities for simulation by providing self-consistent solutions of fields and currents capable of describing dynamic and distributed effects and, thus, eliminating the need for making *a priori* assumptions in circuit level simulations.

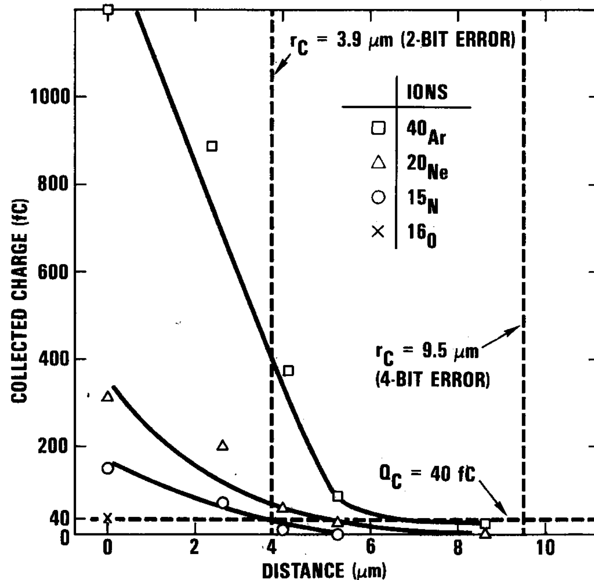

Figure 7. Collected charge as a function of distance

Example Calculation of 4-Bit Error Cross-Section for ^{40}Ar at Normal Incidence

The analysis developed in the previous section provides a method of predicting multiple error cross-sections in the MBU regime. As an example we calculated 4-bit error cross-sections caused by normally incident ^{40}Ar ions. A schematic layout of four adjacent cells in the horizontal plane is shown in Figure 8: cells are arranged on a 10 μm × 20 μm periodic lattice; the four n^+ nodes on the top and bottom represent sensitive drains in the adjacent cells; the two p^+ nodes on the sides represent the p-well contacts. Normally incident ions were simulated as a point source of carriers with spatial profiles given by the TRIPOS-E results [4]. Charge collections on the drains

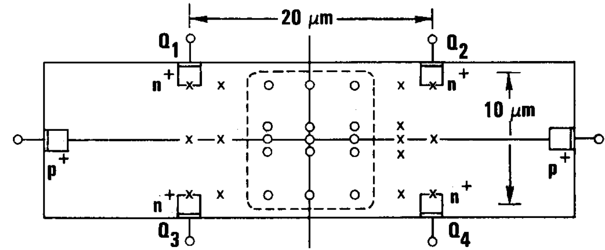

Figure 8. Construction of 4-bit error cross-section for ^{40}Ar

were calculated using the 2-D PISCES in the **horizontal plane**. This method produces a quasi-3-D simulation capability for normal incidence of ions. Since the diffusion equation which governs the motion of carriers in the MBU regime is linear, solving by separation of variables is possible and, for normally incident ions, solutions can be factored into terms involving vertical and horizontal dimension variables only. The normalization of charge density is identical to that in the previous section; the LET threshold for 2-bit errors is 3 $MeV/mg/cm^2$ of ^{15}N. The source strength for ^{40}Ar ions was linearly scaled with LETs from ^{15}N ions.The dotted line in Figure 8 represents the boundary of the 4-bit error cross-section for ^{40}Ar ions: ion hits inside this area, denoted by circles, cause all four n^+ nodes to individually collect more than Q_C; ion hits outside, denoted by x's, do not. The experimentally observed 4-bit error cross-section for ^{40}Ar is 25 μm^2/cell from Figure 4, while the PISCES result gives 40 μm^2/cell. Considering the limitations associated with 2-D codes, the result is satisfactory and seems to support the validity of our approach.

SUMMARY AND CONCLUSIONS

High density NMOS SRAMs with poly-silicon load have been found to be extremely sensitive to SEU. Newly observed phenomena, single-event-induced MBUs, proliferate in this type of device. High pull-up resistances are needed for this type of device to minimize the stand-by current. However, long time constants associated with high pull-up resistances are the primary reason for MBUs. The device is a candidate for high speed computer applications at low space altitudes; this causes concern.

We have developed experimental and analytical methods to investigate in detail the underlying mechanisms of MBU phenomena. Diffusion currents, which have never been a factor in SEU for most other device types, cause bit errors in these NMOS devices. A single ion hit can result in more than one error provided that sufficient engergy is deposited. Ions do not have to make a direct hit on sensitive nodes. The entire chip area can be sensitive to SEU. Error cross-sections defined in the conventional way can actually be larger than the physical dimensions of the chip. The probability of single events approaches unity at relatively low LETs. The conventional approach to SEU analysis, based on the probabilistic concept, may no longer work or at least may not be useful. An acceptable methodology must be developed to define quantitative measures of SEU sensitivities in this regime. A method of calculating realistic error rates in space environments must be devised for this type of device.

Efforts toward the experimental and analytical investigations of these phenomena are just starting. Methods of investigation must be further expanded and refined. For instance, the spatial distribution of multiple errors could be resolved with focused microbeam apparatus. Three dimensional simulations are a necessity for accurate predictions of phenomena. Viable hardening guidelines for these phenomena should be developed based on careful experimental and analytical studies. Junction-type diffusion barriers, for instance, could be used to stop the lateral diffusion in the common well. Periodic refreshing of memory contents may help reduce the problem of long circuit time constants. Similar phenomena may become observable in ultra-large scale CMOS devices, since the diffusion time will scale as the square of the feature size.

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